

ADG619/ADG620
FEATURES

6 Ω (Max) On Resistance
0.8 Ω (Max) On Resistance Flatness
2.7 V to 5.5 V Single Supply
 ± 2.7 V to ± 5.5 V Dual Supply
Rail-to-Rail Operation
8-Lead SOT-23 Package, 8-Lead MSOP Package
Typical Power Consumption (<0.1 μ W)
TTL/CMOS Compatible Inputs

APPLICATIONS

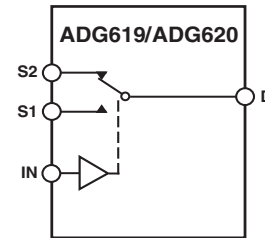
Automatic Test Equipment
Power Routing
Communication Systems
Data Acquisition Systems
Sample-and-Hold Systems
Avionics
Relay Replacement
Battery-Powered Systems

GENERAL DESCRIPTION

The ADG619 and the ADG620 are monolithic, CMOS SPDT (single pole, double throw) switches. Each switch conducts equally well in both directions when on.

The ADG619/ADG620 offer low on resistance of 4 Ω , which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation yet give high switching speeds. The ADG619 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG620 exhibits make-before-break action.

The ADG619/ADG620 are available in an 8-lead SOT-23 package and an 8-lead MSOP package.

FUNCTIONAL BLOCK DIAGRAM


SWITCHES SHOWN FOR A LOGIC 1 INPUT

Table I. Truth Table for the ADG619/ADG620

IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

PRODUCT HIGHLIGHTS

1. Low On Resistance (R_{ON}) (4 Ω typ).
2. Dual ± 2.7 V to ± 5.5 V or Single 2.7 V to 5.5 V Supply.
3. Low Power Dissipation. CMOS construction ensures low power dissipation.
4. Fast t_{ON}/t_{OFF} .
5. Tiny 8-Lead SOT-23 Package and 8-Lead MSOP Package.

REV. A

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ADG619/ADG620—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$. All specifications -40°C to $+85^{\circ}\text{C}$, unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
On Resistance (R_{ON})	4		Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$;
	6	8	Ω max	Test Circuit 1
On Resistance Match between Channels (ΔR_{ON})	0.7		Ω typ	$V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	1.1	1.35	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.7	0.8	Ω typ	$V_S = \pm 3.3\text{ V}$, $I_S = -10\text{ mA}$
	1.15	1.2	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.25	± 1	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	Test Circuit 2
	± 0.25	± 1	nA max	$V_S = V_D = \pm 4.5\text{ V}$; Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS²				
ADG619				
t_{ON}	80		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	155	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
t_{OFF}	45		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	75	90	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
Break-Before-Make Time Delay, t_{BBM}	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$; Test Circuit 5
ADG620				
t_{ON}	40		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	65	85	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
t_{OFF}	200		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	330	400	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
Make-Before-Break Time Delay, t_{MBS}	160		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_S = 0\text{ V}$; Test Circuit 6
Charge Injection	110		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$;
				Test Circuit 7
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 10
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	25		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	95		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
		1.0	μA max	Digital Inputs = 0 V or 5.5 V
I_{SS}	0.001		μA typ	Digital Inputs = 0 V or 5.5 V
		1.0	μA max	

NOTES

¹Temperature range is as follows: B Version, -40°C to $+85^{\circ}\text{C}$.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$. All specifications -40°C to $+85^\circ\text{C}$, unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	$V_{DD} = 4.5\text{ V}$, $V_{SS} = 0\text{ V}$
On Resistance (R_{ON})	7		Ω typ	$V_S = 0\text{ V}$ to 4.5 V , $I_S = -10\text{ mA}$;
	10	12.5	Ω max	Test Circuit 1
On Resistance Match between Channels (ΔR_{ON})	0.8		Ω typ	$V_S = 0\text{ V}$ to 4.5 V , $I_S = -10\text{ mA}$
	1.1	1.3	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.5	0.5	Ω typ	$V_S = 1.5\text{ V}$ to 3.3 V , $I_S = -10\text{ mA}$
		1	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I_S (OFF)	± 0.01		nA typ	$V_{DD} = 5.5\text{ V}$
	± 0.25	± 1	nA max	$V_S = 1\text{ V}/4.5\text{ V}$, $V_D = 4.5\text{ V}/1\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.01		nA typ	Test Circuit 2
	± 0.25	± 1	nA max	$V_S = V_D = 1\text{ V}/4.5\text{ V}$;
				Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2		pF typ	
DYNAMIC CHARACTERISTICS²				
ADG619				
t_{ON}	120		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	220	280	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
t_{OFF}	50		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	75	110	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
Break-Before-Make Time Delay, t_{BBM}	70		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$,
		10	ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$; Test Circuit 5
ADG620				
t_{ON}	50		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	85	110	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
t_{OFF}	210		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	340	420	ns max	$V_S = 3.3\text{ V}$; Test Circuit 4
Make-Before-Break Time Delay, t_{MBB}	170		ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
		10	ns min	$V_S = 3.3\text{ V}$; Test Circuit 6
Charge Injection	6		pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$;
				Test Circuit 7
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
				Test Circuit 10
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Test Circuit 9
C_S (OFF)	25		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	95		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS				
I_{DD}	0.001		μA typ	$V_{DD} = 5.5\text{ V}$
		1.0	μA max	Digital Inputs = 0 V or 5.5 V

NOTES

¹Temperature range is as follows: B Version, -40°C to $+85^\circ\text{C}$.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG619/ADG620

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to V _{SS}	13 V
V _{DD} to GND	-0.3 V to +6.5 V
V _{SS} to GND	+0.3 V to -6.5 V
Analog Inputs ²	V _{SS} - 0.3 V to V _{DD} + 0.3 V
Digital Inputs ²	-0.3 V to V _{DD} + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	50 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ _{JA} Thermal Impedance	206°C/W
θ _{JC} Thermal Impedance	44°C/W
SOT-23 Package	
θ _{JA} Thermal Impedance	229.6°C/W
θ _{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

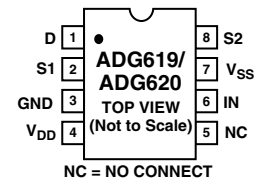
NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

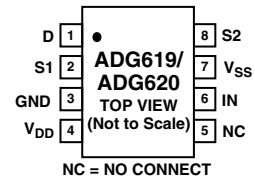
² Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

PIN CONFIGURATIONS

8-Lead SOT-23 (RT-8)



8-Lead MSOP (RM-8)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information*
ADG619BRM	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SVB
ADG619BRM-REEL	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SVB
ADG619BRM-REEL7	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SVB
ADG619BRT-R2	-40°C to +85°C	Plastic Surface Mount Package (SOT-23)	RT-8	SVB
ADG619BRT-REEL	-40°C to +85°C	Plastic Surface Mount Package (SOT-23)	RT-8	SVB
ADG619BRT-REEL7	-40°C to +85°C	Plastic Surface Mount Package (SOT-23)	RT-8	SVB
ADG620BRM	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SWB
ADG620BRM-REEL	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SWB
ADG620BRM-REEL7	-40°C to +85°C	Micro Small Outline Package (MSOP)	RM-8	SWB
ADG620BRT-REEL	-40°C to +85°C	Plastic Surface Mount Package (SOT-23)	RT-8	SWB
ADG620BRT-REEL7	-40°C to +85°C	Plastic Surface Mount Package (SOT-23)	RT-8	SWB

*Branding on SOT-23 and MSOP packages is limited to three characters due to space constraints.

CAUTION

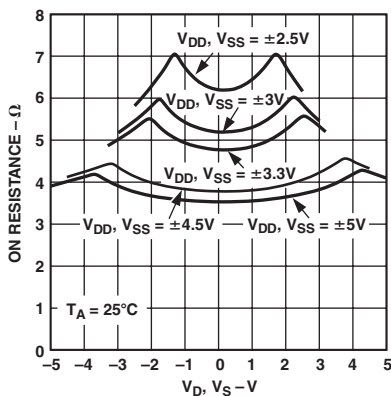
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG619/ADG620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



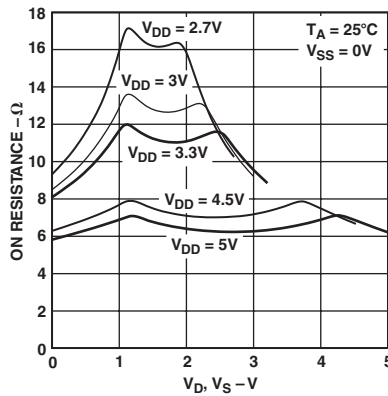
TERMINOLOGY

Mnemonic	Description
V_{DD}	Most Positive Power Supply Potential.
V_{SS}	Most Negative Power Supply in a Dual-Supply Application. In single-supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference.
I_{DD}	Positive Supply Current.
I_{SS}	Negative Supply Current.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R_{ON}	Ohmic Resistance between D and S.
DR_{ON}	On resistance match between any two channels, i.e., $R_{ON} \text{ Max} - R_{ON} \text{ Min}$.
$R_{FLAT} \text{ (ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
$I_S \text{ (OFF)}$	Source Leakage Current with the Switch OFF.
$I_D, I_S \text{ (ON)}$	Channel Leakage Current with the Switch ON.
$V_D \text{ (} V_S \text{)}$	Analog Voltage on Terminals D, S.
V_{INL}	Maximum Input Voltage for Logic 0.
V_{INH}	Minimum Input Voltage for Logic 1.
$I_{INL} \text{ (} I_{INH} \text{)}$	Input Current of the Digital Input.
$C_S \text{ (OFF)}$	OFF Switch Source Capacitance.
$C_D, C_S \text{ (ON)}$	ON Switch Capacitance.
t_{ON}	Delay between applying the digital control input and the output switching ON.
t_{OFF}	Delay between applying the digital control input and the output switching OFF.
t_{MBS}	ON time is measured between the 80% points of both switches, when switching from one address state to another.
t_{BBS}	OFF time or ON time is measured between the 90% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Crosstalk	A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an OFF switch.
Bandwidth	The frequency response of the ON switch.
Insertion Loss	The loss due to the on resistance of the switch.

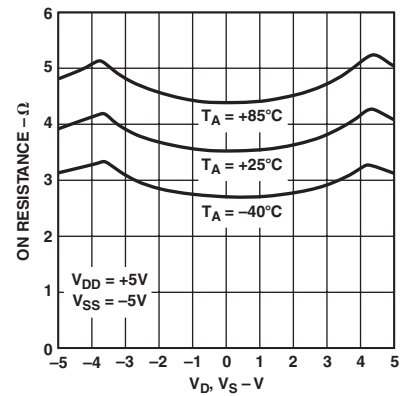
Typical Performance Characteristics



TPC 1. On Resistance vs. $V_D \text{ (} V_S \text{)}$ (Dual Supply)

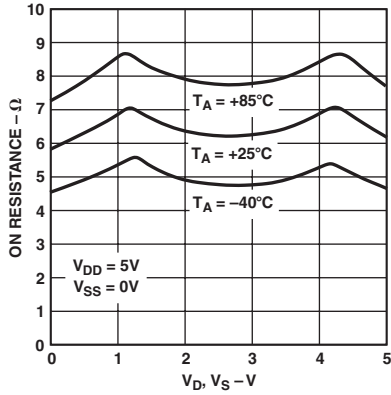


TPC 2. On Resistance vs. $V_D \text{ (} V_S \text{)}$ (Single Supply)

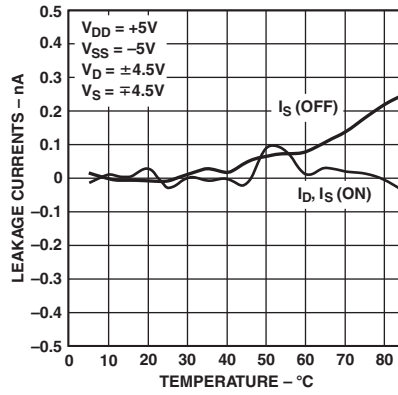


TPC 3. On Resistance vs. $V_D \text{ (} V_S \text{)}$ for Different Temperatures (Dual Supply)

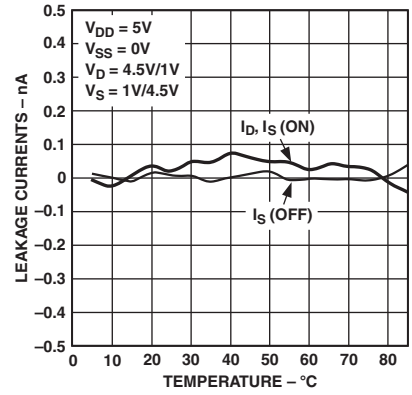
ADG619/ADG620



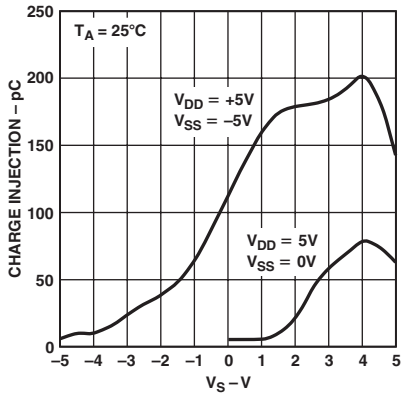
TPC 4. On Resistance vs. V_D (V_S) for Different Temperatures (Single Supply)



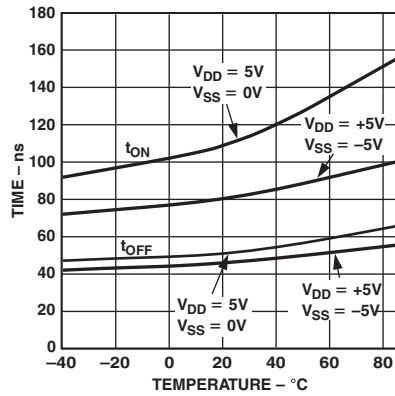
TPC 5. Leakage Currents vs. Temperature (Dual Supply)



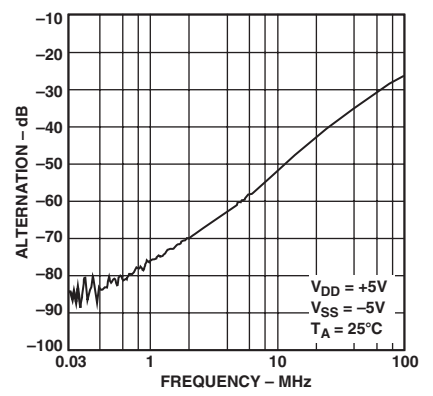
TPC 6. Leakage Currents vs. Temperature (Single Supply)



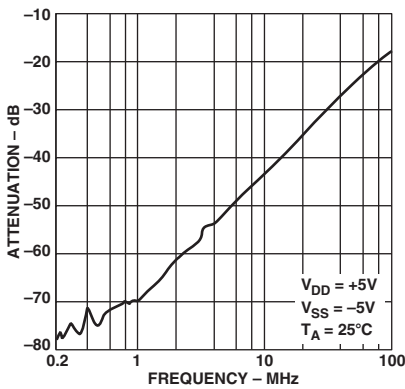
TPC 7. Charge Injection vs. Source Voltage



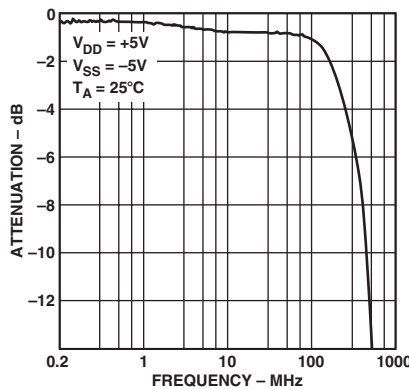
TPC 8. t_{ON}/t_{OFF} Times vs. Temperature



TPC 9. Off Isolation vs. Frequency

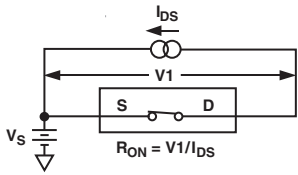


TPC 10. Crosstalk vs. Frequency

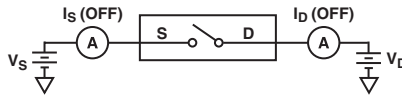


TPC 11. On Response vs. Frequency

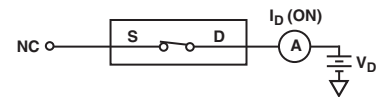
TEST CIRCUITS



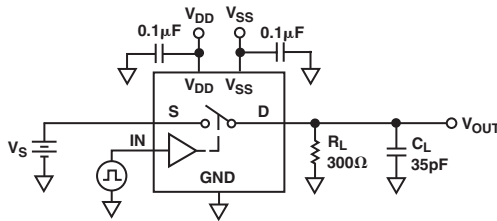
Test Circuit 1. On Resistance



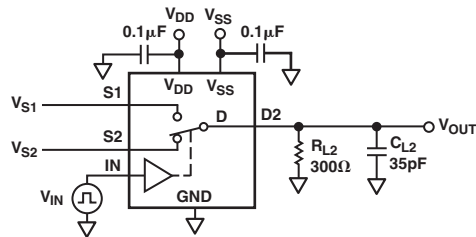
Test Circuit 2. Off Leakage



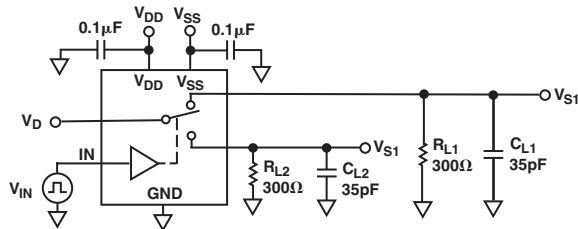
Test Circuit 3. On Leakage



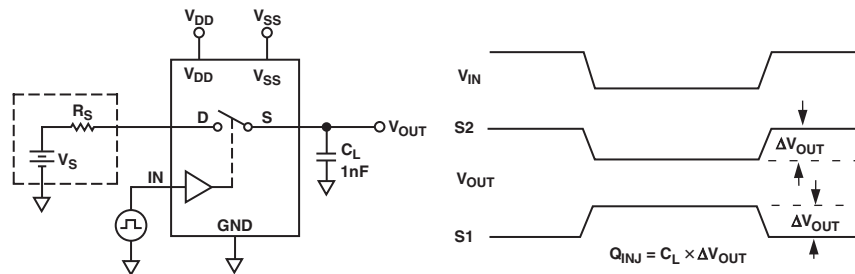
Test Circuit 4. Switching Times



Test Circuit 5. Break-Before-Make Time Delay, t_{BBM} (ADG619 Only)

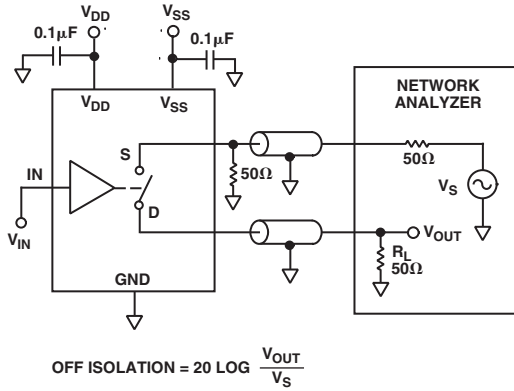


Test Circuit 6. Make-Before-Break Time Delay, t_{MBB} (ADG620 Only)

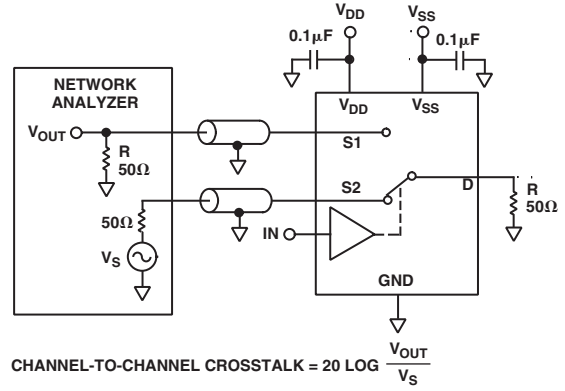


Test Circuit 7. Charge Injection

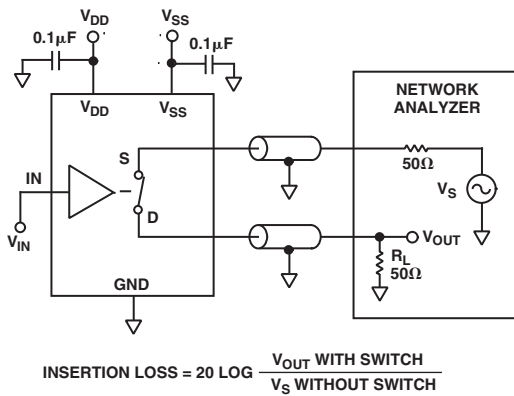
ADG619/ADG620



Test Circuit 8. Off Isolation



Test Circuit 10. Channel-to-Channel Crosstalk

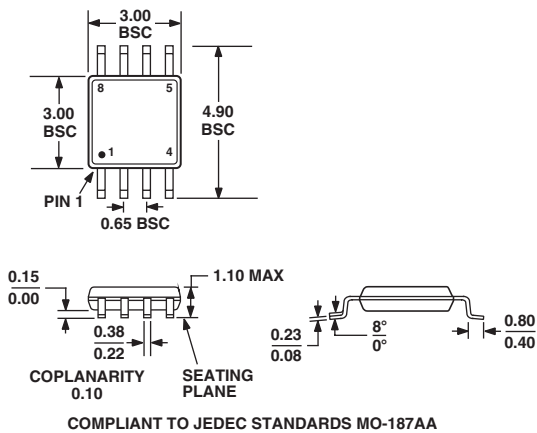


Test Circuit 9. Bandwidth

OUTLINE DIMENSIONS

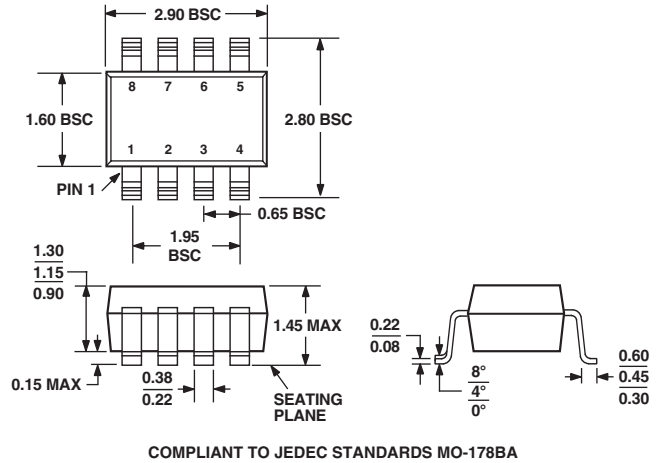
8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



8-Lead Small Outline Transistor Package [SOT-23] (RT-8)

Dimensions shown in millimeters



Revision History

Location	Page
6/03—Data Sheet changed from REV. 0 to REV. A.	
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Updated ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	8